UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,431	11/28/2003	Takayuki Kondo	117603	7372

25944 7590 08/24/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
PEACE, RHONDA S	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,431	KONDO, TAKAYUKI	
	Examiner	Art Unit	
	Rhonda S. Peace	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,8,9 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,8,9 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 8 is objected to because of the following informalities: Claim 8 recites the following: "at least part of the optical waveguide covering being at least one of the first element and the third element." The wording of claim 8 implies the waveguide covering is a concrete object that covers the waveguide. However, claim 16 introduces no such "waveguide covering." Instead it is believed that the scope of claim 8 is to describe a waveguide orientation where the waveguide covers at least one of the first or third elements, and has been examined under such an assumption. Appropriate correction is required.

Claim 13 is objected to because of the following informalities: Claim 13, which is directly dependent upon claim 16, recites the phrase "wavelength multiplexing on-chip optical interconnection circuit." However, claim 16 simply refers to the current invention as "an optical interconnection circuit." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2-6, 8, 9, and 12-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda (US 6430325) in further view of Chraplyvy et al (US 6205268)

Pertaining to claims 16, 18, 19, 21, and 23, Shimoda discloses an optical interconnection circuit comprising the following:

- An integrated circuit chip, such as a LSI circuit or a TFT circuit (column 13 lines 38-43, hereafter indicated as 13:38-43).
- A first circuit block **81(A)** provided on the integrated chip, and having a first light emitting element **301** and a first light receiving element **502** (13:44-52, Fig 13), where the first light emitting element **301** may emit a light having a wavelength λ_1 (14:29-34) and is driven by a first driving circuit **11** (13:44-51). The first light-receiving element **502** is driven by circuit **602** (13:44-51).
- A second circuit block **82(B)** provided on the integrated chip, and having a second light emitting element **302** and a second light receiving element **501** (13:44-52, Fig 13), where the second light emitting element **302** may emit a light having a wavelength λ_2 (14:29-34) and is driven by a second driving circuit **12** (13:44-51). The second light-receiving element **501** is driven by circuit **601** (13:44-51).

In addition, Shimoda discloses a waveguide **401** that optical couples the first light-emitting element **301** to the second light-receiving element **501**, and likewise waveguide **402** optical couples the second light emitting element **302** to the first light receiving element **502** (13:53-60, Fig 13). However, Shimoda does not disclose an optical waveguide that optical connects the entire plurality of elements.

Further pertaining to claims 16, 18, 19, 21, and 23, Chraplyvy et al discloses a high capacity optical fiber network **100** having waveguide **130** which optically couples a plurality of light emitters **101**, **111-1**, **111-4**, **121-1**, and **121-16** to a plurality of light

receivers **105**, **115-1**, **115-4**, **125-1**, and **125-16** such that signals of various wavelengths (1.3 microns, 1.4 microns, and 1.55 microns) may be bi-directionally sent along waveguide **130** (5:15-24 and 28-31, Fig 1). It would have been obvious to one of ordinary skill in the art to combine the teachings of Shimoda and Chraplyvy et al, as transmitting several wavelengths along the same optical fiber allows for the device of Shimoda to eliminate several waveguides (as all signals can be transmitted on a single guide as opposed to a plurality of guides), thereby minimizing the cost, size, and production time associated with the device, and also allows for a more reliable optical connection between the circuit blocks, as only one waveguide must be optically coupled between the blocks as opposed to many.

Addressing claims 2 and 6, Shimoda, in view of Chraplyvy et al, disclose the device as described above. In addition, Shimoda discloses the circuit blocks **81(A)** and **82(B)** are optically connected to one another, for example through waveguide **401** (13:53-56, Fig 13), and are also electrically connected to one another (see abstract, 14:14-17). Moreover, Shimoda discloses the first light receiving element **301** is electrically connected to the first circuit block **81(a)** via the driving circuit **11**; second light emitting element **302** is electrically connected to the second circuit block **82(B)** via the driving circuit **12**; first light receiving element **502** is electrically connected to the first circuit block **81(A)** via the driving circuit **602**; second light receiving element **501** is electrically connected to the second circuit block **82(B)** via the driving circuit **601** (13:44-51, Fig 13).

Regarding claims 14 and 15, Shimoda, in view of Chraplyvy et al, disclose the device as described above. Furthermore, Shimoda discloses the device described above can both convert electrical signals to optical signals (such as at light transmitter **301**, see 13:44-47) and transmit electrical signals to the integrated circuit (such as through amplifying circuit **601**, see 14:14-17, 7:66-67, 8:1-5), the device described above may be considered (in and of itself) both an electro-optical device and an electrical device, and therefore any apparatus incorporating a device as described above would also be considered both an electro-optical and an electrical apparatus.

Pertaining to claims 3-5 and 8, Shimoda, in view of Chraplyvy et al, disclose the device as described above. Notice that in Figure 13, Shimoda shows the waveguide **401** as being placed between the circuit blocks **81(A)** and **82(B)**. While this is the only orientation shown for the waveguide **401**, it would have been obvious to one of ordinary skill in the art to fashion the waveguide **401** in various other manners, as Shimoda explains that the waveguide **401** may also be fashioned in two and three-dimensional orientations (14:62-67, 15:1-6). The important feature of the waveguide **401** is that it optically connects the first circuit block **81(A)** to the second circuit block **82(B)**. Any manner by which this optical connection is accomplished, whether *a portion the waveguide is provided on the top surfaces of the circuit blocks and transmitters and/ or receivers (so as to cover them), or a portion of the waveguide is provided on the circuit blocks so as to traverse them, or a portion of the waveguide is provided to detour the circuit blocks*, is considered obvious to one of ordinary skill in the art due to the possible two and three dimensional (in addition to the one dimensional) waveguide orientations

discussed by Shimoda (14:62-67, 15:1-6). In addition, modification of the waveguide from the orientation shown in Figure 13 would allow the device to be further refined to optimize optical connection between the two circuit blocks and minimize size, thereby improving overall performance and applicability of the device.

Addressing claim 9, Shimoda, in view of Chraplyvy et al, disclose the device as described above. However, Shimoda does not disclose the specific use of a *CPU, memory circuit, DSP, RF amplifying circuit, image sensor, or biosensor as the circuit blocks* ***81(A) and 82(B).*** However, it would have been obvious to one of ordinary skill in the art to use any of the above circuits as the circuit blocks **81(A)** and **82(B),** as all are well known components which may act as circuit blocks, and in addition, further specification of the components of the device as described by Shimoda will allow the device to be applied to several differing applications

Regarding claims 12 and 13, Shimoda, in view of Chraplyvy et al, disclose the device as described above. Moreover, Shimoda's device described above may be applied to optical signal transmission between circuit blocks **81(A)** and **82(B)**, where the plurality of circuit blocks are formed on two separate semiconductor chips (14:35-45), thereby allowing the chips to be optically connected. Shimoda does not disclose *mounting these communicating semiconductor chips on a common substrate, or tightly bonding the chips to one another.* However, it would have been obvious to one of ordinary skill in the art to mount the communicating chips on a common substrate so that the optical waveguides connecting the circuit blocks of differing chips can be mounted upon the common substrate, thereby allowing for a more reliable optical

connection between the circuit blocks. It would also have been obvious to one of ordinary skill in the art to bond the chips tightly to one another, as this will further decrease the size of the overall device making it more applicable to compact applications, as well as further ensuring a reliable optical connection between the chips.

Pertaining to claim 17, Shimoda, in view of Chraplyvy et al, disclose the device as described above. In addition, Shimoda discloses the above device may further include a plurality of light emitting elements on the first circuit block **81(A)**, and a plurality of light receiving elements on the second circuit block **82(B)** (15:1-3). As the second light receiver **501** (on **82(B)**) receives the first light from first light emitter **301** (on **81(A)**) along waveguide **401**, so would a third light receiver (on **82(B)**) receive a second light from a second light emitter (on **81(A)**) via a waveguide separate from waveguide **401**, where the first and second lights may be of differing wavelengths, as discussed above.

With respect to claim 20, Shimoda, in view of Chraplyvy et al, disclose the device as described above. Moreover, Shimoda discloses each circuit block, such as the first **81(A)**, may contain a plurality of light emitters (13:44-52, 15:1-3). Figure 13 illustrates an embodiment showing only one light emitter **301** on the first circuit block **81(A)**. Emitter **301** is driven by a first driving circuit **11** (13:44-52), and therefore similar light emitters placed on the first circuit block **81(A)** would also be driven by an additional circuit similar to driving circuit **11**.

Regarding claim 22, Shimoda, in view of Chraplyvy et al, disclose the device as described above. Shimoda includes that a first emitter **301** (on first circuit block **81(A)**

will emit a first light which is then received by a second receiving element **501** on the second circuit block **82(B)** (13:53-60, Fig 13). Similarly, an additional (or second) light emitter provided on first circuit lock **81(A)** would transmit a second light to an additional (or second) light-receiving element provided on the second circuit block **82(B)** (13:61-67, 15:1-3). As the light receiving element **501** is driven by a (third) circuit **601** (13:44-51), any additional light receiving elements provided on the second circuit block **82(B)** would also be driven by their own circuit similar to circuit **601**. As discussed above, Chraplyvy et al discloses a waveguide that may replace the waveguides of Shimoda so that all signals may be transmitted bi-directionally along a common waveguide for the reasons discussed above.

Response to Arguments

Applicant's arguments, see pages 9-12, filed 6/30/2006, with respect to the rejection(s) of claim(s) 16 under 35 U.S.C. §102(e), and the rejection(s) of claim(s) 19 under 35 U.S.C. §103(a) over Shimoda in view of White, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shimoda in further view of Chraplyvy et al, as discussed above.

Applicant's arguments, see page 9, filed 6/30/2006, with respect to the rejection(s) of claim(s) 8, 12, and 22 under 35 U.S.C. §112 have been fully considered and are persuasive. The 35 U.S.C. §112 rejection of claim(s) 8, 12, and 22 has been withdrawn.

Applicant's arguments, see page 9, filed 6/30/2006, with respect to the objection of claims 2-6, 8, 9, 11, 12, 14, and 15 have been fully considered and are persuasive. The objection of claims 2-6, 8, 9, 11, 12, 14, and 15 has been withdrawn.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda S. Peace whose telephone number is (571) 272-8580. The examiner can normally be reached on M-F (8-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272- 2344. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Rhonda S. Peace
Examiner
Art Unit 2874

John D. Lee
Primary Examiner